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| EWULogo.png | | **EAST WEST UNIVERSITY** | |
| **Department of Computer Science and Engineering** | |
| **B.Sc. in Computer Science and Engineering Program** | |
| **Mid Term II Examination, Summer 2022** | |
| **Course:** | | **CSE360 – Computer Architecture, Section 3** | |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Professor, CSE Department** | |
| **Full Marks:** | | **25** | |
| **Time:** | | **1 Hour 20 Minutes** | |
| **Note:** There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin. | | | |
| 1. | A four-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 128-Mbyte main memory is byte addressable. Show the format of main memory addresses. | | [ CO2, C3, Mark: 3] |
| 2. | Consider a memory system with the following parameters:  Tc = 236 ns Cc = 10^-2 $/ bit  Tm = 2268 ns Cm = 10^-3 $/ bit  a) What is the cost of 4.25 MB of main memory using cache memory technology?  b) If the effective access time is 17% greater than the cache memory access time, what is the miss ratio? | | [CO2, C2, Mark:1+3] |
| 3. | Consider a magnetic disk drive having the following specifications   |  |  | | --- | --- | | Rotational speed | 7500 rotations /minute | | Bytes/track | 1500 bytes /track | | Average seek time | 45 milliseconds |  1. What is the average rotational latency? 2. What is the data transfer rate? 3. What is the average access time for reading a data block 3500 bytes? | | [ CO2, C5, Mark: 2+2+3] |
| 4. | Examination of the timing diagram of the 8237A indicates that once a block transfer begins, it takes eight clock cycles per DMA cycle. During the DMA cycle, the 8237A transfers two bytes of information between memory and I/O devices.   1. Suppose clock speed of 8237A is 640 MHz How long does it take to transfer one byte of data? 2. What would be the maximum attainable data transfer rate? 3. What will be the actual data transfer rate if we insert two wait states per DMA cycle? | | [ CO2, C4, Mark: 2+3+3] |
| 5. | A 128-bit computer has four selector channels and one multiplexor channel. Each selector channel supports three magnetic disk and two magnetic tape units. The multiplexor channel has three-line printers, four card readers, and 11 VDT terminals connected to it. Assume the following transfer rate:  Disk drive: 450 Kbytes/sec  Magnetic tape drive 200 Kbytes/sec  Line printer 2.6 Kbytes /sec  Card reader: 3.1 Kbytes/sec  VDT: 2.35 Kbytes/sec  Estimate the minimum aggregate I/O transfer rate in this system. | | [ CO2, C4, Mark:3] |
| 6. | A hard disk has 600 cylinders, 40 tracks per cylinder, 60 sectors per track and 1KB can be stored in one sector. What is the capacity of the hard disk? | | [CO2, C3, Mark: 2] |